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10/788,420	03/01/2004	Richard Paul Brandwein JR.	044499-0198	4964

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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,420	BRANDWEIN, RICHARD PAUL	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Remarks

1. Applicant's arguments with respect to claims 1-4, 10, 12-16 and 18-23 have been considered but are moot in view of the new grounds of rejection.

Specification

2. The disclosure is objected to because of the following informalities:

Page 6, paragraph 31, lines 1 and 4, the resistor 112 should be corrected to 122 according to figure 5 and the description in paragraph 0030.

Page 6, paragraph 0032, line 1 and paragraph 0034, line 1, the resistor 212 and 213 should be corrected to 222 and 223 according to figure 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, and 10-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art of the instant application discloses in figure 1 and paragraph 0004-0005 (admitted prior art) in view of Luff et al. (US 7,076,217 B1).

(1) Regarding claim 1:

The admitted prior art of the instant application discloses a method of deriving a reference voltage for a data slicer comprising:

supplying a signal to a filter and filtering the signal (signal from the ASK/FSK switch 16 is supply to the low pass filter 14 and filtered by low pass filter 14, paragraph 0005, lines 1-3);

supplying the filtered signal to a comparator which comprises the data slicer (the filtered signal from the low pass filter 14 is supply to the comparator 18, paragraph 0005, lines 3-5);

passing the signal prior filtering through an RC circuit (the signal prior to the low pass filter 14 is pass to the RC circuit comprising R and C through a capacitor in figure 1); and

using the output of the RC circuit as the reference voltage for the comparator (the threshold voltage from the RC circuit is applied to the comparator 18 which function as a data slicer, paragraph 0005, lines 8-9).

The admitted prior art fails to disclose amplifying the signal before the step of filtering the signal.

However, Luff et al. discloses a receiver portion of a transceiver (figure 1) that amplifies the signal before passing the signal to the demodulator that may be a discriminator and data slicer (the IF amplifier 12 increase the IF signal level before being processed by the demodulator 14).

It is desirable to amplifier the signal before the step of filtering the signal because it increase the IF signal level for proper demodulation the signal (column 4, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Luff et al. in the method of admitted prior art to correctly demodulate the signal and improve the performance of the method.

(2) Regarding claim 2:

The admitted prior art of the instant application discloses that the filter is a low pass filter (low pass filter 14 in figure 1, paragraph 0005, lines 1-3).

(3) Regarding claim 3:

The admitted prior art of the instant application discloses wherein the data slicer forms part of a cascaded RF receiver system (paragraph 0002, lines 1-3 and paragraph 0003, lines 1-3).

(4) Regarding claim 4:

The admitted prior art of the instant application discloses wherein the signal is an IF (Intermediate Frequency) signal (since the current invention is an improvement to the prior art base on the same PLL IC, therefore the signal in the prior art is an IF (Intermediate Frequency) as in the current invention, paragraph 0020, lines 1-5).

(5) Regarding claim 5:

The admitted prior art of the instant application discloses a method of deriving a reference voltage for a data slicer comprising:

supplying a signal to a filter and filtering the signal (signal from the ASK/FSK switch 16 is supply to the low pass filter 14 and filtered by low pass filter 14, paragraph 0005, lines 1-3);

supplying the filtered signal to a comparator which comprises the data slicer (the filtered signal from the low pass filter 14 is supply to the comparator 18, paragraph 0005, lines 3-5);

passing the signal prior filtering through an RC circuit (the signal prior to the low pass filter 14 is pass to the RC circuit comprising R and C through a capacitor in figure 1); and

using the output of the RC circuit as the reference voltage for the comparator (the threshold voltage from the RC circuit is applied to the comparator 18 which function as a data slicer, paragraph 0005, lines 8-9).

The admitted prior art fails to disclose wherein the signal is an IF (intermediate frequency) signal and the frequency of the signal is up to about 4KHz.

However, according to the specification of the instant invention (paragraph 0035), the limitation of the signal up to 4KHz is perform by choosing the resistor value of resistor 122 and 123 to 300 ohm and 30 ohm respectively. Since the admitted prior art discloses the same internal circuit as figure 5, it is inherent that the circuit in figure 1 can perform the same function as the circuit discloses in figure 5.

(6) Regarding claim 10:

The admitted prior art discloses method comprising:

supplying the modulated IF signal to a first filter circuit and a second filter circuit (the signal from the ASK/FSK switch 16 is supply to the low pass filter 14 and the RC filter circuit in external stage 12 as shown in figure 1);

supplying a first filtered signal from the first filter to a comparator as a data signal (the output of the low pass filter 14 is supply to the comparator 18 as a data input, paragraph 0005, lines 3-5); and

supplying a second filtered signal from the second filter to the comparator as a reference voltage for the comparator (the threshold voltage from the RC circuit is applied to the comparator 18 which function as a slicer, paragraph 0005, lines 8-9).

The admitted prior art fails to disclose amplifying the signal before the step of filtering the signal.

However, Luff et al. discloses a receiver portion of a transceiver (figure 1) that amplifies the signal before passing the signal to the demodulator that may be a discriminator and data slicer (the IF amplifier 12 increase the IF signal level before being processed by the demodulator 14).

It is desirable to amplifier the signal before the step of filtering the signal because it increase the IF signal level for proper demodulation the signal (column 4, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Luff et al. in the method of admitted prior art to correctly demodulate the signal and improve the performance of the method.

(7) Regarding claim 12:

The prior art of the instant application discloses wherein the second filter is a low pass filter (the RC circuit in the external stage of 12 of figure 1 form a low pass filter circuit).

(8) Regarding claim 13:

The prior art of the instant application discloses wherein the second filter is an RC circuit (the RC circuit in the external stage of 12 of figure 1 form a low pass filter circuit).

(9) Regarding claim 11:

The admitted prior art discloses method comprising:

supplying the modulated IF signal to a first filter circuit and a second filter circuit (the signal from the ASK/FSK switch 16 is supply to the low pass filter 14 and the RC filter circuit in external stage 12 as shown in figure 1);

supplying a first filtered signal from the first filter to a comparator as a data signal (the output of the low pass filter 14 is supply to the comparator 18 as a data input, paragraph 0005, lines 3-5); and

supplying a second filtered signal from the second filter to the comparator as a reference voltage for the comparator (the threshold voltage from the RC circuit is applied to the comparator 18 which function as a slicer, paragraph 0005, lines 8-9).

The admitted prior art fails to disclose the modulated IF signal is an amplified IF signal.

However, Luff et al. discloses a receiver portion of a transceiver (figure 1) that amplifies the signal before passing the signal to the demodulator that may be a

discriminator and data slicer (the IF amplifier 12 increase the IF signal level before being processed by the demodulator 14).

It is desirable to amplifier the signal before the step of filtering the signal because it increase the IF signal level for proper demodulation the signal (column 4, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Luff et al. in the method of admitted prior art to correctly demodulate the signal and improve the performance of the method.

(10) Regarding claim 14:

The admitted prior art of the instant application discloses a circuit comprising:

a source of an IF frequency signal for demodulation (the IF frequency signal from the ASK/FSK switch 16 in figure 1);

a filter and a comparator serially connected with the source (the low pass filter 14 and the comparator 18 is serially connected with the source as shown in figure 1, paragraph 0005, lines 1-5); and

a reference voltage circuit (the RC circuit in the external stage 12 of figure 1) connected to the comparator and configured to produce a comparator reference voltage (threshold voltage of the RC circuit), the reference voltage circuit comprising a resistor and a capacitor (R and C in the external stage of figure 1), the resistor being connected to a point between the source and the filter (the resistor R is connected to the point between the ASK/FSK switch 16 and low pass filter 14 through a capacitor as shown in figure 1) so as to be responsive a signal which is being supplied to the filter (the signal

supply to the low pass filter 14 is pass through a capacitor and connect to the resistor R).

The admitted prior art fails to disclose wherein the signal is amplified before being input into the filter.

However, Luff et al. discloses a receiver portion of a transceiver (figure 1) that amplifies the signal before passing the signal to the demodulator that may be a discriminator and data slicer (the IF amplifier 12 increase the IF signal level before being processed by the demodulator 14).

It is desirable to amplifier the signal before the step of filtering the signal because it increase the IF signal level for proper demodulation the signal (column 4, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Luff et al. in the method of admitted prior art to correctly demodulate the signal and improve the performance of the method.

(11) Regarding claim 15:

The prior art of the instant application discloses wherein the source of the IF frequency signal comprises an ASK/FSK switch (ASK/FSK switch 16 as discloses in figure 1, paragraph 0005, lines 1-3).

(12) Regarding claim 16:

The prior art of the instant application discloses wherein the source of an IF frequency signal, filter and comparator serially connected with the source, comprise elements of an internal stage of a chip (as discloses in figure 1, the ASK/FSK switch 16, the low pass filter 14 and the comparator 18 are connected in series and all of them are

within the internal stage 11, the internal stage 11 represents sealed within the chips, paragraph 0004, lines 3-5 and paragraph 005, lines 1-5).

(13) Regarding claim 18:

The admitted prior art of the instant application discloses wherein the capacitor of the reference voltage circuit comprises part of an external stage of the chip (as shown in figure 1, the capacitor C of the reference voltage circuit comprises part of an external stage 12 of the chip, paragraph 0004, lines 7-9).

(14) Regarding claim 19:

The admitted prior art of the instant application discloses wherein the resistance and the capacitor of the reference voltage circuit comprise parts of the external stage of the chip (as shown in figure 1, the resistor R and the capacitor C are in the external stage 12, paragraph 0004, lines 7-9).

(15) Regarding claim 20:

The admitted prior art of the instant application discloses a circuit comprising:

a source of an IF frequency signal for demodulation (the IF frequency signal from the ASK/FSK switch 16 in figure 1);

a filter and a comparator serially connected with the source (the low pass filter 14 and the comparator 18 is serially connected with the source as shown in figure 1, paragraph 0005, lines 1-5); and

a reference voltage circuit (the RC circuit in the external stage 12 of figure 1) connected to the comparator (the RC circuit in the external stage 12 is connected to the comparator 18) and configured to respond to a signal having a component which is

comparable with a component filtered by the filter (the RC reference voltage circuit receives a signal before filtering through a capacitor and a signal after filtering as shown in figure 1).

The admitted prior art fails to disclose wherein the signal is amplified before being input into the filter.

However, Luff et al. discloses a receiver portion of a transceiver (figure 1) that amplifies the signal before passing the signal to the demodulator that may be a discriminator and data slicer (the IF amplifier 12 increase the IF signal level before being processed by the demodulator 14).

It is desirable to amplifier the signal before the step of filtering the signal because it increase the IF signal level for proper demodulation the signal (column 4, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Luff et al. in the method of admitted prior art to correctly demodulate the signal and improve the performance of the method.

(16) Regarding claim 21:

The prior art of the instant application discloses wherein the circuit forms part of a wireless communication device (as it states in paragraph 0002, the present invention relates generally to a receiver circuit for use in devices such as keyless entry receiver circuit, it indicates that the prior art discloses in figure 1 is also generally related to the same kind of application, which is a wireless communication device).

(17) Regarding claim 22:

The prior art of the instant application discloses wherein the wireless communication device comprises a keyless entry system for an automotive vehicle (for the same reason as states in claim 21 above, it is obvious to one of ordinary skill in the art at the time of invention to apply the keyless entry receiver circuit for an automotive vehicle).

(18) Regarding claim 23:

The prior art of the instant application discloses wherein the wireless communication device comprises a tire pressure monitoring system for an automotive vehicle (for the same reason as states in claim 21 above, it is obvious to one of ordinary skill in the art at the time of invention to apply the keyless entry receiver circuit for a tire pressure monitor system for an automotive vehicle).

(19) Regarding claim 17:

The admitted prior art discloses a circuit comprising:

a source of an IF frequency signal for demodulation (the IF frequency signal from the ASK/FSK switch 16 in figure 1);

a filter and a comparator serially connected with the source (the low pass filter 14 and the comparator 18 is serially connected with the source as shown in figure 1, paragraph 0005, lines 1-5);

a reference voltage circuit (the RC circuit form by the resistor R3 and the capacitor C in figure 1) connected to the comparator (the RC circuit form by the resistor R3 and the capacitor C is connected to the comparator 18) and configured to produce a comparator reference voltage (the signal input to the comparator from the capacitor C),

the reference voltage circuit comprising a resistor (resistor R3 in figure 1) and a capacitor (capacitor C in figure 1), the resistor being connected to a point between the source and the filter so as to be responsive to a signal which is being supplied to the filter (the resistor R3 is connected to a point between the source and the filter through R2 so as to be responsive to a signal which is being supplied to the filter),

wherein the source of an IF frequency signal, filter and comparator serially connected with the source (the block 16, 14 and 18 in figure 1 is serially connected with the source as shown in figure 1), comprise element of an internal stage of a chip (the internal stage in figure 1 is an integrated circuit) and the resistor of the reference voltage circuit is an internal element of the chip (resistor R3 is an internal element of the chip (inside the internal stage)).

5. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art of the instant application discloses in figure 1 and paragraph 0004-0005 (admitted prior art) in view of Vilhonen et al. (US 6,972,633 B2).

Regarding claim 7, 8, and 9:

The admitted prior art of the instant application discloses a method of deriving a reference voltage for a data slicer comprising:

supplying a signal to a filter and filtering the signal (signal from the ASK/FSK switch 16 is supply to the low pass filter 14 and filtered by low pass filter 14, paragraph 0005, lines 1-3);

supplying the filtered signal to a comparator which comprises the data slicer (the filtered signal from the low pass filter 14 is supply to the comparator 18, paragraph 0005, lines 3-5);

passing the signal prior filtering through an RC circuit (the signal prior to the low pass filter 14 is pass to the RC circuit comprising R and C through a capacitor in figure 1); and

using the output of the RC circuit as the reference voltage for the comparator (the threshold voltage from the RC circuit is applied to the comparator 18 which function as a data slicer, paragraph 0005, lines 8-9).

The admitted prior art fails to disclose adjusting a value of a capacitor comprising the RC circuit or adjusting the value of a resistor of a RC circuit or adjusting the value of at least one of a resistor and a capacitor of the RC circuit in order to modulate the reference voltage supplied to the comparator.

However, Vilhonen et al. discloses an method of adjusting the a value of a capacitor of a RC filter circuit or adjusting the value of a resistor of a RC circuit or adjusting the value of at least one of a resistor and a capacitor of the RC circuit in order to modulate the reference voltage supplied to the comparator (RC-filter component includes at least one of a tunable resistor and a tunable capacitor, and wherein said calibrating component tunes said at least one RC-filter component of said loop-filter by changing at least the value of said tunable resistor and/or the value of said tunable capacitor of said at least one RC-filter component of said loop-filter, column 6, lines 1-8).

It is desirable to adjusting the a value of a capacitor of a RC filter circuit or adjusting the value of a resistor of a RC circuit or adjusting the value of at least one of a resistor and a capacitor of the RC circuit because it can calibrate the RC filter and provide flexibility for adjusting the characteristics of the filter. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Vilhonen et al. in the method of the admitted prior art to increase the flexibility of the method.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mikhael et al. (US 3,891,938) discloses a functionally tunable active low pass filter. Lee et al. (US 2002/0106038 A1) discloses a data slicer and RF receiver employing the same. Porat et al. (US 7,149,243 B2) discloses a system and method for establishing an XDSL data transfer link. Ravatin et al. (US 6,525,568 B2) discloses a circuit for the demodulation of the logic signal transmitted by analog channels.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M Lee
Examiner
Art Unit 2611
10/3/2007

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SUPERVISORY PATENT EXAMINER